What is claimed is:

1. A method for testing signals of integrated circuits (ICs), comprising the steps of:

successively driving, by a first IC chip, a plurality of test patterns one at a time;

receiving, at a second IC chip, and latching in the test patterns on by one;

determining, by the second IC chip, whether a currently latched test pattern is correct;

if at least an error bit occurs in the currently latched test pattern, the second IC chip indicating that there exists noise interference in a signal trace corresponding to the error bit; and

repeating the above steps until the first IC chip finishes driving the test patterns.

2. The method of claim 1 wherein the test patterns are at least divided into three types including a ground bounce type, a power bounce type and a heavy load type.

3. The method of claim 2 further comprising the step of:

if the currently latched test pattern is incorrect, the second IC chip adjusting a reference voltage level in accordance with the type of the corresponding test pattern to change an input threshold of the second IC chip.

4. The method of claim 3 wherein the reference voltage level is decreased to lower the input threshold of the second IC chip if the corresponding test pattern belongs to the power bounce type.

5. The method of claim 3 wherein the reference voltage level is increased to raise the input threshold of the second IC chip if the corresponding test pattern belongs to the ground bounce type.

6. The method of claim 3 wherein the reference voltage level is adjusted in a unit of 0.01 volts at a time.

7. The method of claim 3 wherein the reference voltage level is adjusted by changing an internal register setting of the second IC chip.

8. The method of claim 1 further comprising the step of:

adjusting a driving capability of a pin relative to the error bit for the first IC chip to change the pin's output timing.

9. The method of claim 8 wherein the driving capability of the pin relative to the error bit is increased to advance the pin's output timing for the first IC chip.

10. The method of claim 8 wherein the driving capability of the pin relative to the error bit is decreased to delay the pin's output timing for the first IC chip.

11. The method of claim 8 wherein the output timing is changed in a unit of 150 ps at a time when adjusting the pin's driving capability for the first IC chip.

12. The method of claim 8 wherein the output timing is adjusted by changing an internal register setting of the first IC chip.

13. A method for testing signals of integrated circuits (ICs), comprising the steps of:

receiving a plurality of test patterns and latching in the test patterns on by one through an agent in the integrated circuits;

determining, by the agent, whether a currently latched test pattern is correct; and

if at least an error bit occurs in the currently latched test pattern, the agent indicating that there exists noise interference in a signal trace corresponding to the error bit.

14. The method of claim 13 wherein the test patterns are at least divided into three types including a ground bounce type, a power bounce type and a heavy load type.

15. The method of claim 14 further comprising the step of:

if the currently latched test pattern is incorrect, the agent in the integrated circuits adjusting a reference voltage level in accordance with the type of the corresponding test pattern to change an input threshold of the agent.

16. The method of claim 15 wherein the reference voltage level is decreased to lower the input threshold of the agent if the corresponding test pattern belongs to the power bounce type.

17. The method of claim 15 wherein the reference voltage level is increased to raise the input threshold of the agent if the corresponding test pattern belongs to the ground bounce type.

18. The method of claim 15 wherein the reference voltage level is adjusted in a unit of 0.01 volts at a time.

19. The method of claim 15 wherein the reference voltage level is adjusted by changing an internal register setting of the agent.

20. The method of claim 15 further comprising the step of:

adjusting a driving capability of a pin relative to the error bit for the agent to change the pin's output timing.

21. The method of claim 20 wherein the driving capability of the pin relative to the error bit is increased to advance the pin's output timing for the agent.

22. The method of claim 20 wherein the driving capability of the pin relative to the error bit is decreased to delay the pin's output timing for the agent.

23. The method of claim 20 wherein the output timing is changed in a unit of 150 ps at a time when adjusting the pin's driving capability for the agent.

24. The method of claim 20 wherein the output timing is adjusted by changing an internal register setting of the agent.